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PRELIMINARY AMENDMENT AND RESPONSE TO
RESTRICTION REQUIREMENT MAILED APRIL 28, 2003)

PATENT

AMENDMENTS TO THE CLAIMS

A1

1. (Currently Amended) A method of forming a dual-sided semiconductor device from a wafer, the wafer having a ~~top~~ first surface, a ~~bottom~~ an opposing second surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material on the ~~top~~ first surface of the wafer;
 patterning the layer of masking material to ~~form a first opening in the layer of masking material that exposes~~ expose a first region on the ~~top~~ first surface; and
 forming a ~~first~~ an opening in the wafer and a doped region in the wafer ~~between the first opening in the wafer and the bottom side after the layer of masking material has been patterned, the opening forming exposed regions of the wafer,~~ the doped region having a ~~top~~ surface exposed by the first opening in the wafer, and a dopant concentration that is greater than the dopant concentration of the wafer;
~~forming a layer of conductive material to fill up the first opening in the wafer;~~
and
~~planarizing the layer of conductive material to form a first conductive region directly over the doped region.~~

2. (Currently Amended) The method of claim 1 ~~wherein 21 and~~
further comprising the steps of:

~~the forming a layer of masking material is also formed on the bottom second surface of the wafer, the layer of masking material is patterned to form a second opening in the layer of masking material that exposes to expose~~ a second region on the ~~bottom second~~ surface of the wafer, the first and second openings regions being substantially vertically aligned,

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a second forming an opening is formed in the bottom side second surface of the wafer; to expose the doped region in the wafer being between the first and second openings in the wafer after the layer of masking material has been patterned, the doped region having a bottom surface exposed by the second opening in the second surface of the wafer; and

the forming a layer of conductive material is formed to also fill up the second opening in the second surface of the wafer; and

the layer of conductive material is also planarized to form a second conductive region directly below that contacts the doped region.

3. (Currently Amended) The method of claim 2 21 wherein the step of forming a first an opening in the wafer and a doped region in the wafer includes the steps of:

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

introducing a dopant into the wafer through the first and second openings in the layer of masking material regions, the dopant extending continuously through the wafer from the first region to the second region, and forming a continuous region through the wafer that has a dopant concentration greater than a dopant concentration of the wafer; and

etching the first and second regions for a predetermined period of time after the dopant has been introduced to define the a first opening in the top first surface of the wafer, the a second opening in the bottom second surface of the wafer, and the doped region there between.

4. (Currently Amended) The method of claim 2 21 wherein the step of forming a first an opening in the wafer and a doped region in the wafer includes the steps of:

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forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

introducing a dopant into the wafer through the first and second openings in the layer of masking material regions, the dopant extending continuously through the wafer from the first region to the second region;

removing the layer of masking material after the dopant has been introduced;

forming a protective layer on the top first surface and the bottom second surface of the wafer after the layer of masking material has been removed;

patterning the protective layer to form a first opening in the protective layer that exposes expose the first region of the top first surface, and a second opening in the protective layer that exposes the second region of the bottom second surface, the first and second openings in the protective layer being substantially aligned; and

etching the first and second regions for a predetermined period of time after the protective layer has been patterned to define the a first opening in the top side first surface of the wafer, the a second opening in the bottom side second surface of the wafer, and the doped region there between.

5. (Currently Amended) The method of claim 2 21 wherein the step of forming a first an opening in the wafer and a doped region in the wafer includes the steps of:

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

etching the first and second regions for a predetermined period of time to define the a first opening in the top first surface of the wafer, the a second opening in the bottom second surface of the wafer, and a remaining region there between; and

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introducing a dopant into the wafer through the first and second openings in the layer of masking material, the dopant extending continuously through the remaining region to form the doped region.

6. (Currently Amended) The method of claim 2 21 wherein the step of forming a first an opening in the wafer and a doped region in the wafer includes the steps of:

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

etching the first and second regions for a predetermined period of time to define the a first opening in the top first surface of the wafer, the a second opening in the bottom second surface of the wafer, and a remaining region there between;

removing the layer of masking material after the etch has been completed;

forming a protective layer on the top first surface and the bottom second surface of the wafer after the layer of masking material has been removed;

patterning the protective layer to form a first opening in the protective layer that exposes a top surface of the remaining region, and a second opening in the protective layer that exposes a bottom surface of the remaining region, the first and second openings in the protective layer being substantially aligned; and

introducing a dopant into the wafer through the first and second openings in the protective layer, the dopant extending continuously through the remaining region.

7. (Currently Amended) The method of claim 2 21 and further comprising the step of forming a first diffusion barrier on the doped region and exposed regions of the wafer, wherein the layer of conductive material is formed on the first diffusion barrier to fill up the first and second openings in the wafer.

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8. (Cancel).

9. (Original) The method of claim 2 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the second conductive region.

10. (Currently Amended) The method of claim ~~4~~ 21 wherein the doped region has a surface substantially planar with the ~~bottom~~ second surface of the wafer.

11. (Currently Amended) The method of claim 10 wherein the step of forming ~~a~~ first an opening in the wafer and a doped region in the wafer includes the steps of:

introducing a dopant into the wafer through the ~~first opening in the layer of masking material region~~, the dopant extending continuously through the wafer from the ~~top~~ first surface of the wafer to the ~~bottom~~ second surface of the wafer; and

etching the first region for a predetermined period of time after the dopant has been introduced to define the ~~first~~ opening in the ~~top~~ surface of the wafer, and the doped region between the ~~first~~ opening and the ~~bottom~~ second surface of the wafer.

12. (Currently Amended) The method of claim 10 wherein the step of forming ~~a~~ first an opening in the wafer and a doped region in the wafer includes the steps of:

etching the first region for a predetermined period of time to define the ~~first~~ opening in the ~~top side of the~~ wafer, and a remaining region between the ~~first~~ opening and the ~~bottom~~ second surface; and

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introducing a dopant into the wafer ~~through the first opening in the layer of masking material~~, the dopant extending continuously through the remaining region to form the doped region.

13. (Original) The method of claim 10 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the doped region.

14. (Original) The method of claim 10 and further comprising the step of forming a contact through the doped region to make an electrical connection with the first conductive region.

15. (Original) The method of claim 14 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the contact.

Claims 16-20. (Cancel).

21. (New) The method of claim 1 and further comprising the step of forming a layer of conductive material to fill up the opening in the wafer and form a first conductive region that contacts the doped region.